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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(use as many sheets as necessary)</i>			Application Number	
			Filing Date	
			First Named Inventor	Alter, Martin
			Art Unit	
			Examiner Name	
			Attorney Docket Number	M085
Sheet	1	of	2	

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FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No. 1	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T 6
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Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T <sup>2</sup>
		GARROU, Wafer-Level Packaging Has Arrived, Semiconductor International, Oct. 2000, 119 et seq  YOUNG, Wafer-level Processing, May 1997, Chip Scale Review, May 1997, 28 et seq.  NGUYEN et al., Assembly Considerations for SMD Wafer-Level CSPs, Chip Scale Review, May/June 2000, 48 et seq.  CHAN et al., Integrated Antennas on Si,..., IEDM 10-903, 0-7803-7050-3/01/\$10.00 copr. 2001 IEEE, 40.6.1 et seq.  PENNWELL CORP., Is THIS the industry's next killer app?, <a href="http://sst.pennnet.com/Articles/">http://sst.pennnet.com/Articles/</a> , ... 7/14/2003, 7pp.  LIHUI et al., High Q Multilayer Spiral Inductor on Silicon Chip for 5-6 GHz, IEEE Electron Device Letters, Vol. 23, No. 8, August 2002, 470 et seq.	

Examiner Signature	Date Considered
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